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Appeal Brief
Dequp
11/25/02

Docket No.: GR 97 P 1903

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By: _____ Date: November 4, 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applicant : Hansjörg Reichert et al.

Applic. No. : 09/483,737

Filed : January 14, 2000

Title : Method and Apparatus for Producing a Chip-Substrate Connection

Examiner : Ahmed N Sefer - Art Unit: 2826

BRIEF ON APPEAL

Hon. Commissioner of Patents and Trademarks,
Washington, D. C. 20231,

S i r :

This is an appeal from the final rejection in the Office action dated May 3, 2002, finally rejecting claims 15 and 17.

Appellants submit this Brief on Appeal in triplicate, including payment in the amount of $320.00 to cover the fee for filing the Brief.

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Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 15 and 17 are rejected and are under appeal. Claims 1-10 are withdrawn from further consideration. Claims 11-14 and 16 were cancelled in an amendment filed February 19, 2002.

Status of Amendments:

No claims were amended after the final Office Action. A *Response under 37 CFR § 1.116* was filed on August 5, 2002. The Primary Examiner stated in an *Advisory Action* dated August 20, 2002, that the request for reconsideration had been considered but did not place the application in condition for allowance.

Summary of the Invention:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention relates to a method and an apparatus for producing a chip-substrate connection by alloying or brazing, using a solder with two metal-containing constituents X and Y, the first constituent X containing in particular gold or a similar precious metal. The invention furthermore relates to a solder for the production of a chip-substrate connection, and to a semiconductor component with a semiconductor chip which is secured to a substrate by alloying or brazing.

Appellants explained on page 7 of the specification, line 18, that, referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown that for an AuSn composition the eutectic temperature is 278° Celsius, and a specific composition contains 20% Sn and 80% Au (percent by weight). Therefore, alloy formation takes place at a temperature that lies well below the melting temperature of the individual components. In accordance with the fundamental concept of the invention, an AuSn solder with a hypereutectic concentration of tin is used, so that the AuSn solder contains more than 20% by weight Sn. The result is a sufficiently low viscosity of the solder at temperatures of below 380° Celsius for mounting in surface mounting

devices or SOT housings, since diffusion of Sn into adjoining layers of metal causes the composition of the AuSn to move away from the tin-rich phase toward the eutectic point, so that a gold-rich solder phase which lies above the eutectic is avoided. The melting temperature of the AuSn mixture rises very steeply if Au is in excess, while the increase in the melting point is significantly less if the mixture is enriched with Sn. A loss of Sn from an Sn-rich solder according to the invention results in a continuous reduction in the melting point during the soldering operation, thus promoting the soldering operation. The melting temperature is reduced locally in particular at the contact point between solder and a lead frame (for example Ag), where the Sn depletion takes place, thus improving the flow properties of the solder. For this reason, an excess supply of Sn results in reproducible mounting conditions at low temperatures. This effect is greatly emphasized in particular in the case of thin layers of solder, as are conventionally used when coating the rear side of wafers.

Appellants outlined on page 8 of the specification, line 23, that Figs. 2A and 2B show a connection between a semiconductor chip 1 on a central "island" 2 of a metallic lead frame 3, which is produced by alloying or brazing. The prefabricated metallic lead frames 3 represent a very

widespread form of substrate, in particular for use in plastic housings. The enlarged partial view shown in Fig. 2B shows the sequence of layers in more detail. A rear side of the semiconductor chip 1 is provided with an adhesion or diffusion barrier 4, which preferably contains Ti/Pt. Reference numeral 5 denotes a layer of solder that has been sputtered onto the rear side of the wafer with a thickness of typically 1.5 µm. To allow the chip-substrate connection to have a sufficiently low resistance, it may be necessary for a doping layer, for example of AuAs, or a contact implantation 6 also to have been incorporated beforehand.

References Cited:

U.S. Patent No. 5,234,153 (Bacon et al.), dated August 10, 1993;

U.S. Patent No. 6,245,208 B1 (Ivey et al.), dated June 12, 2001;

Published Japanese Patent Application No. 2-15897 (Komata et al.), dated January 19, 1990;

Published Japanese Patent Application No. 6-291239 (Yamagishi et al.), dated October 18, 1994.

Issues

1. Whether or not claims 15 and 17 are obvious over Yamagishi et al. in view of Komata et al. and Bacon et al. under 35 U.S.C. §103(a).

2. Whether or not claims 15 and 17 are obvious over Yamagishi et al. in view of Ivey et al. and Bacon et al. under 35 U.S.C. §103(a).

Grouping of Claims:

Claim 15 is independent. Claim 17 is dependent on claim 15. The patentability of claim 17 is not separately argued. Therefore, claim 17 stands or falls with claim 15.

Arguments:

In item 3 on pages 2-3 of the above-mentioned final Office action dated May 3, 2002, claims 15 and 17 have been rejected as being unpatentable over Yamagishi et al. in view of Komata et al. and Bacon et al. under 35 U.S.C. § 103(a).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 15 calls for, inter alia:

said solder containing a gold-tin compound (AuSn) with a hypereutectic Sn concentration and forming a layer having a thickness of from about 1 µm to about 2 µm.

Yamagishi et al. disclose a gold-tin soldered joint between the housing 5 of a semiconductor chip 4 and a substrate 1, on which lead pins 2 are connected (see Fig. 1(c)). However, Yamagishi et al. do not disclose a connection of the chip 4 with the pins 2 or the pads 3 and the chip 4. Such a connection is also hardly realistic at that location, because the substrate 1 apparently should have a considerable layer thickness.

Therefore, the important feature of the invention of the instant application, namely the direct connection of a semiconductor body with a substrate over a thin gold-tin solder layer with a hypereutectic Sn concentration and a layer thickness of 1-2 µm, is not disclosed by Yamagishi et al. The same also applies to the other cited references.

Komata et al. disclose a hypereutectic gold-tin-alloy with a tin content of 12-37% by weight (see page 585, left column, middle). However, as can be clearly seen from the drawings of Komata et al., such gold-tin-alloy cannot be used together with a semiconductor body.

Bacon et al. disclose a gold-tin solder layer 24 (75% gold and 25% tin by weight) with a layer thickness of about 5μm between a nickel-tin layer 23 and a gold layer 13 in a laser device (see column 5, lines 36-61 and column 6, lines 44-46). A semiconductor chip 10 of the laser device is clearly distant from those layers 13, 24, 23, because additional layers 11, 12 and an ohmic contact layer 10.5 are disposed therebetween. The layer 11 is made of titanium, whereas the layer 12 has platinium.

Clearly, none of the references discloses the important feature of the invention of the instant application, namely the direct joint of a semiconductor chip with a substrate through a hypereutectic gold-tin-alloy having a layer thickness of about 1-2μm. Therefore, the combination of references cannot show that feature.

The invention of the instant application for the first time enables the direct attachment of a chip on a substrate through a thin gold-tin solder joint. The layer thickness of the gold-tin solder layer is at least 2.5 times less than the thickness disclosed in Bacon et al. In Yamagishi et al., there is no solder layer between the semiconductor chip 4 and the substrate 1 or between the semiconductor chip 4 and the housing 5.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 15. Claim 15 is, therefore, believed to be patentable over the art and since claim 17 is dependent on claim 15, it is believed to be patentable as well.

In item 4 on pages 3-4 of the above-mentioned Office action, claims 15 and 17 have been rejected as being unpatentable over Yamagishi et al. in view of Ivey et al. and Bacon et al. under 35 U.S.C. § 103(a).

As discussed above, neither Yamagishi et al. nor Bacon et al. show the essential feature of claim 15, namely the direct joint of a semiconductor chip with a substrate through a hypereutectic gold-tin-alloy having a layer thickness of about 1-2μm.

Applicants respectfully believe that the reference Ivey et al. is not prior art with respect to the instant application. The instant application is a continuation of copending international application **PCT/DE98/01737**, filed **June 24, 1998**. Pursuant to 35 U.S.C. § 363, the instant application has a filing date of **June 24, 1998**, because the instant

application designated the United States. This date is prior to Ivey et al.'s U.S. filing date. Accordingly, the reference Ivey et al. is unavailable as prior art.

Therefore, applicants respectfully submit that the rejection in item 4 on pages 3-4 of the Office action under Section 103(a) is moot.

In view of the foregoing, the honorable Board is respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

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Appendix - Appealed Claims:

15. A semiconductor component, comprising:

a solder containing at least two components with at least two metal-containing constituents including a first constituent X being formed of a precious metal and a second constituent Y being consumed during a soldering operation by one of reacting and being dissolved in materials which are to be joined, and said solder having a hypereutectic concentration of said second constituent Y;

a substrate; and

a semiconductor chip secured to said substrate by one of alloying and brazing using said solder,

said solder containing a gold-tin compound (AuSn) with a hypereutectic Sn concentration and forming a layer having a thickness of from about 1 μm to about 2 μm.

17. The semiconductor component according to claim 15, wherein said solder has a composition by weight of said first constituent X to said second constituent Y of 70 to 30.